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Comparison of bulk driven, floating gate and sub threshold methods in designing of a typical amplifier

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ABSTRACT: Nowadays one of the most important parameters in designing analog circuits or even in the digital circuits is Reducing the consumption power of the circuit. In analog circuits, power consumption has a direct relationship with the values of circuit supply voltage and given the equation $P = V_{load} \times C \times f_{ddclk}^2$in digital circuits the power can be directly related to the square of the supply voltage value. It is therefore concluded that the reduction of power consumption of analog or digital circuits can be achieved by reducing the supply voltage. Another advantage of low supply voltage is that circuits are easy to transport because the small battery is used as the supply voltage on them. (e.g., audio devices).

***Keywords*:** electronic amplifier, bulk driven, floating gate, sub threshold, power consumption, low voltage supply, CMOS, HSPICE.

INTRODUCTION

In the industry it is tried to reduce the electronic tools size for easier access to them such as audio devices including mobile. One of the ways to reduce the volume is using the low supply voltage. Because in doing so In addition to reducing the volume of the produced part, its power consumption will also be reduced. Although a reduced supply voltage is suitable to achieve this goal but there are limits to the threshold voltage of transistors and so that the supply value cannot be reduced. However, several methods have been proposed through which one can achieve to a voltage gain and appropriate margin with minimal supply voltage, among them there are sub-threshold, bulk-driven, floating gate that each has strengths and pitfalls. in the paper it is tried to compare 3 methods in order to deal with their strengths and pitfalls therefore a double floor circuit has been proposed which all mentioned methods have been used in order to design it to reach a 35 dB gain with 6 V supply .then in the next sections we have tried to compare the results considering briefly each method the intended circuit will be designed finally.

Floating gate MOSFET

Please Floating gate MOSFET has a structure similar to a conventional MOSFET. The only difference between the control gate and its substrate is that there is a poly silicon floating gate which is surrounded by an insulating silicon dioxide. (Blalock and Allen, 1995; Tai, 2006).

Gure 2.1 shows the structure of an N-channel floating gate MOSFET with two inputs &. The circuit analysis of this MOSFET is similar to an incremental MOSFET the only difference is that the inputs are connected to the transistor gate as capacitor connection. The symbol of the device is shown in Figure 1. The capacitors & are symbol of formed capacitors between the floating gate and input gates and is the capacitor between the floating

gate and body. The performance of the device is similar to a conventional MOSFET, which the only difference with the conventional MOSFET is that the voltage on the gate is not directly controlled by the input control but the inputs can control the voltage on the gate via capacitors & .. The transistors can also work in active and sub-threshold area based on voltage relationship between gate and source and threshold voltage value.
if transistor works in The active region. $(V_{FG,S} \geq V_{THeq})$

$$V_{theq} = \frac{c_1 + c_2 + c_0}{c_1} V_{th} - \frac{c_2}{c_1} V_2 \quad (1)$$

$$C_0 \prec\prec C_2 \Rightarrow$$

$$V_{theq} = V_{th} + \frac{c_2}{c_1}(V_{th} - V_2) \quad (2)$$

$$I_D = \frac{\beta w}{2l}(v_{FG,S} - v_t)^2 \quad (3)$$

$$v_{FG} = \begin{pmatrix} Q_{FG} + C_{FG,D} V_D + C_{FG,S} V_S \\ + C_{FG,B} V_B + \sum_{i=1}^{n} C_{Gi} V_{Gi} / C_T \end{pmatrix} \quad (4)$$

$$C_T = C_{FG,S} + C_{FG,D} + C_{FG,B} + \sum_{1}^{n} C_{Gi} \quad (5)$$

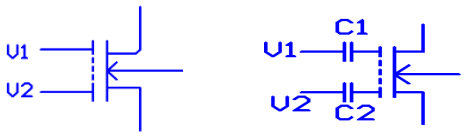
$$g_m = k g_{mFG} \quad (6)$$

However, if the transistor works in the active area , we will have the following equation: and source and threshold voltage value.

$$V_{FG,S} \geq V_{THeq} \quad g_m = k \cdot I_D \quad (7)$$

Thus via a floating gate transistor the total threshold voltage of the device can be lowered by applying a DC voltage (Razavi, 2001; Bahmani and Fakhraie, 2000). We'll dim the threshold voltage by selecting values of the input capacitors even by selecting appropriately k2 and v1 we can reach the value Vth to zero. Its small signal model is shown in Figure 2.

The capacitor between gate and drain causes the output impedance of the transistor is reduced and the circuit gain dimed.



(A) (B)

Figure 1. floating-gate MOSFET model

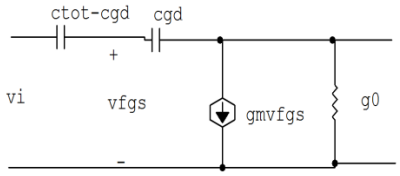


Figure 2. Small signal model of MOSFET floating gate

$$g_{0f} = \left(\frac{C_{GD}}{C_T}\right) g_m + g_0 \quad (8)$$

The transistor has various applications in the circuit .Due to insulator between floating gate the other nodes the load on it can be maintained for long periods of time. For this reason its important application is to make EPROM and EEPROM memories in digital circuits.

In analog circuits because the amount of threshold voltage of transistors can be controlled and reduced they are used in low voltage circuits. Input capacitance can cause an increase in circuit noise which is eliminated via suitable methods. The major disadvantage of transistors is the high cost during construction. (Rosenfeld and Kozak, 2004; Norman and Neff, 2008; Yang and Andrrou, 2009).

A Brief Study on the sub-threshold method

When the gate - source voltage of a MOSFET transistor is less than the threshold voltage , the Channel is in weak inversion which the area of the performance is called sub-threshold transistor.

Device consumption current in the region is an exponential equation:

$$I_{DS} = \frac{2K^{''}w}{l}\left(\frac{nK_T}{q_e}\right)\exp\left[\frac{q(v_{GS}-v_{tn})}{nk_T}\right] \quad (9)$$

$$g_m = \frac{I_D}{nK_T/q} \quad (10)$$

$$r_0 \cong \frac{1}{\lambda I} \quad (11)$$

In this region because the amount of transistors current is very low, circuit consumption power will below and also voltage drop on the drain - source terminal is low. Because of these two above important properties in designing the low voltage and power circuits this structure is used. Nearly Similar to a transistor BJT, MOSFET transistor trans-induction is directly related to the transistor current in the sub-threshold area (Rosenfeld and Kozak, 2004) Because in the sub-threshold area there is low transistor current so the trans-induction value is low too. But given the gain value is equal to , it is clear that the channel length plays an important role in the operation thus due to channel length increase the gain value will rise. But its weakness is that due to very low transistor current the trans-induction value of transistor is very small , as a result the gain width and extent of circuit is reduced Because - for example - in a two-floor circuit , the value of circuit single gain width is directly related to the value of input floor trans-induction given the equation (14). Therefore, this type of circuit is used in the low frequency.

$$GBW = \frac{g_m}{c_c} \quad (12)$$

In this method we make use of the auxiliary and folded cascade circuit with it to strengthen further gain.

This structure has pitfalls including:

1 It has no a good frequency response.

2 For The values $V_{DS} \prec 3kT/q$,the equations g_m & r_0 are non-linear and makes it difficult to design.

3 To increase the gain of a transistor the devices width should be high and so the speed of the circuit will be reduced.

Investigation of body-driven circuits

Dependency of the threshold voltage to the body voltage

Usually the body terminal voltage in some cases is named as source of error. But the reality is that although the body terminal and the voltage on which and even the voltage deference between this terminal and especially the source terminal create some problems in designing and probably calculation and we should care about it as a second gate for this and even apply input signal to it and expect the signal amplification by the device in these conditions. Given that different discussions set forth for the arrangements with gate input (gate-driven) such as voltage amplification value , frequency response quality , input & output voltage limit, etc. It is necessary to adopt that whether the body can be as input, the above discussion should investigated. The chapter aims to learn more about transistor circuits with signal input to the body terminal (Bulk - Driven), and exploring some important features of amplifier.

with respect to the threshold voltage relations in the devices PMOS, NMOS:

$$g_{mbs} = -\frac{\delta ID}{\delta V_s B} = -(\frac{\delta_{iD}}{\delta V_{Th}})(\frac{\delta V_{TH}}{\delta V_s B}) \qquad (13)$$

$$g_m = -\frac{\delta ID}{\delta V_{GS}} = -(\frac{\delta_{iD}}{\delta V_{Th}})$$

$$\frac{\delta_{V_{TH}}}{\delta_{VSB}} = \frac{\gamma}{2\sqrt{2\varphi f + V_{SB}}}$$

$$V_{TH} = V_{th0} - \gamma(\sqrt{2\varphi f - V_{SB}} - \sqrt{2\varphi f}) \qquad \text{PMOS} \qquad (14)$$

$$I_D = \mu_n C_{ox} \frac{w}{2l}(V_{GS} - V_{th})^2 \qquad (15)$$

$$V_{TH} = V_{th0} + \gamma(\sqrt{2\phi f + V_{SB}} - \sqrt{2\phi f}) \qquad \text{NMOS}$$

It can be seen that the rate of voltage changes of body-source may impact on the threshold voltage. For example, as shown in Figure 3 due to increase of the body terminal voltage in relation to the source, threshold voltage is reduced. Thus, given the drain current relationship with threshold voltage reduction the drain current increases. Another point is presumable from equations (15),(16) and (17) is that the rate of changes of transistors current is less than that of body-source voltage in comparison to that of source-gate voltage , So when the devices are being used up by the body-driven method they have more input changes than gate –driven state . The quality of the above mentioned matter is shown in Figure 3.

According to Figure 3 in a transistor, n-type increases due to increase in the body voltage relative to the transistor current source.

But what is important is that the body terminal voltage value should also be limited because pad lock or leakage current through device internal diodes will effect on the transistor function.

If the input voltage of the body (in the device NMOS) increases, internal bonds PN between the body and source and that of the drain and body source will become active and even activates the links (Figure 4). In addition unwanted BJT transistors may be activated and pad locking happen.

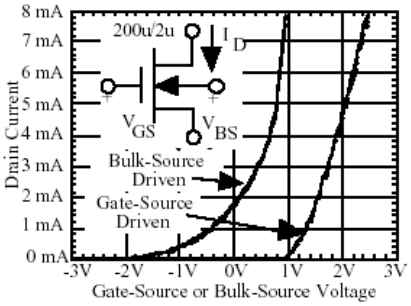


Figure 3. the drain current with respect to body-source and gate - source voltage

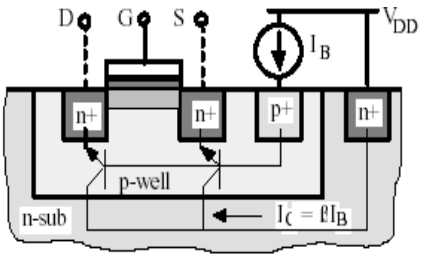


Figure 4. internal structure of an NMOS

In DC analysis of transistor circuit , the drain current can be calculated via following equation regardless of any arrangement.

$$ID = \mu_0 C_{ox} \frac{w}{2l}\left[V_{GS} - V_{TH0} - \gamma\left(\sqrt{2\varphi f + V_{SB}} - \sqrt{2\varphi f}\right)\right]^2 \quad (16)$$

Which the following equations are defined in:

Saturation region

$$V_{DS} \succ V_{GS} - V_{TH} \quad (17)$$

Triode region

$$V_{DS} \prec V_{GS} - V_{TH} \quad (18)$$

Cut-off region

$$V_{GS} \prec V_{TH} \quad (19)$$

So the DC voltage of body - source terminal has a feature either in circuits(Bulk-Driven) or in circuits (Gate-Driven) and will change the operating point to the same extent .In Small-signal analysis of a device as body-driven or with gate input or observing small signal model of the amplifiers we will have the following equations .

Latch up:

$$g_{mbs} = g_m \times \frac{\gamma}{2\sqrt{2\varphi f + V_{SB}}} = \eta g_m \quad (20)$$

$$g_{mbs} = -\frac{\delta ID}{\delta V_s B} = -\left(\frac{\delta_{iD}}{\delta V_{Th}}\right)\left(\frac{\delta V_{TH}}{\delta V_s B}\right) \quad (21)$$

$$g_m = -\frac{\delta ID}{\delta V_{GS}} = -\left(\frac{\delta_{iD}}{\delta V_{Th}}\right) \quad (22)$$

$$\frac{\delta_{V_{TH}}}{\delta_{VSB}} = \frac{\gamma}{2\sqrt{2\varphi f + V_{SB}}}$$

$$0.2 \prec x \prec 0.4 \quad (23)$$

$$V_{BS} \geq 2\phi f - 0.25\gamma^2 \cong 0.5V \quad (24)$$

In The small-signal analysis, the drain current in addition to dependency on the gate - source small signal voltage (V_{gs}) is depended as well to the Body - source small-signal voltage that the dependency value g_m and g_{mbs} is defined via trans-inductions & which in the equations described if $V_{BS} \geq 2\phi f - 0.25\gamma^2 \cong 0.5V$, g_{mbs} is more than g_m , but the pitfall of this is the high leakage current and probably the pad locking Relations (Phillip, 2003). As it has been shown in the above equations $g_{m\,bs} = \eta g_m$, this means that the trans-induction value g_m could even be five times larger than that of trans-induction g_{mbs} .i.e. The value of the signal strength by inserting the input into the body is 5 times lower than signal insertion into the gate, and then it is also the weakness of body-driven circuit .

Another weakness with the body input is its speed reduction relative to the moment the same device works with input gate frame (Pease Robert, 2000).

$$f_{t\,bulk-driven} = \frac{\eta}{3.8} f_{t\,gate-driven} \quad (25)$$

Comparison of methods

Figures 5 ,6 and 7 are respectively the circuits with quite similar structure which their differences are: how to insert the input voltage to the circuit, how to bias and also kind of input transistor. The circuit K in the first floor is a PMOS differential double floor circuit that was used.

The second floor circuit is a low voltage amplification AB. a voltage source was used to bias the second floor circuit. We examine 3 parameters such as size ,phase margin and consumption power to compare the methods for

achieving the voltage gain in 35 dB. Figure 5-1 shows the circuit with differential pair input in the body-driven layout.

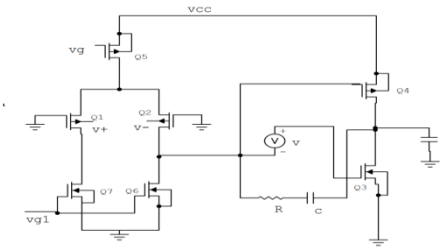


Figure 5. The circuit with body-driven input

Table 1. Size of circuit transistors and elements in figure 5

M	L(µ)	W(µ)
M1	1	1.7
M2	1	1.7
M3	1	4.8
M4	1	8
M5	1	2
M5	1	2
M7	1	7

elements	Size
CL	5p
R	0.1k
C	10n
AV	35db
PH	75
P(w)	946n
elements	Size

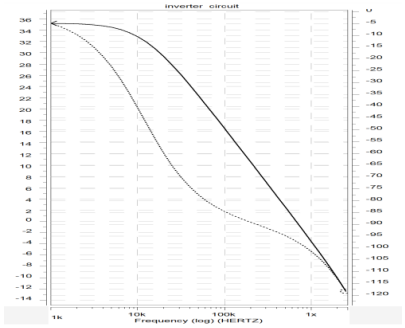


Figure 6. Frequency response of the circuit in Figure 5

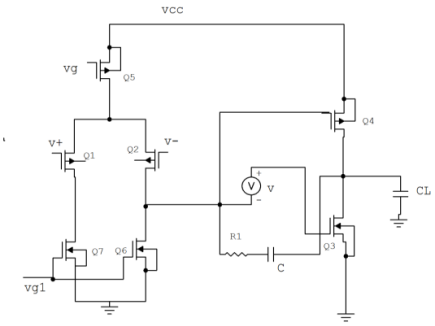


Figure 7. the proposed circuit which all devices are biased in sub-threshold region

Table 2. The transistors and elements size of the circuit in Figure 7

M	L(µ)	W(µ)
M1	10	170
M2	10	170
M3	2	70
M4	2	60
M5	2	40
M6	2	40
7	2	5

elements	Size
CL	5p
C	1.3p
R	200K
AV	35db
PH	30
P(w)	611n

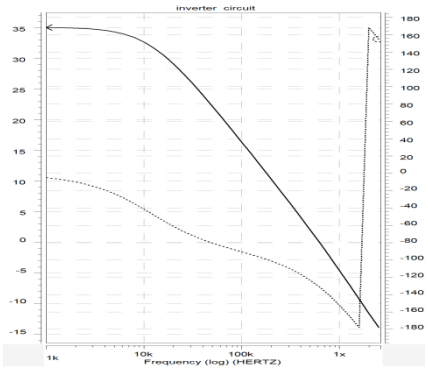


Figure 8. Frequency response of the circuit in Figure 7

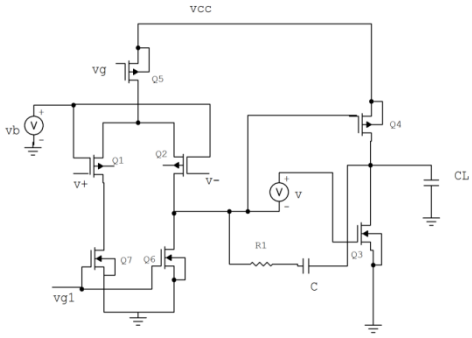


Figure 9. Circuit with floating gate input

We will discuss the circuit via floating gate transistor inputs.

Table 3. Size of the transistors and elements of circuit in Figure 9

M	L(μ)	W(μ)
M1	2	15
M2	2	15
M3	2	12.5
M4	2	2
M5	2	5
M5	2	5
M7	2	5

elements	Size
CL	5p
C	1f
R	0.5K
AV	35db
PH	82
P(w)	1.97u

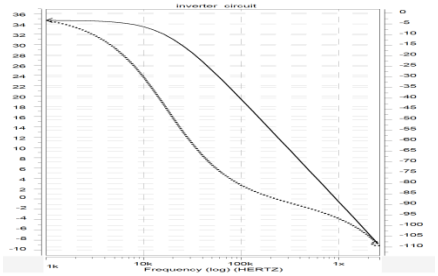


Figure 10. Frequency response of the circuit in Figure 9

It can be seen that in Comparison of phase margin and circuit size (occupied space) the body –driven is more preferred and the sub-threshold method will occupy more volume.

In comparison of power consumption three methods are perceived. The sub-threshold method has less consumption power in proportion to two other methods and the floating-gate method will have more consumption power.

CONCULSION

In the paper after designing a double floor circuit by 3 methods which has been carried out through 6 V supply voltage; it was evident that even if all of them can be used in low supply voltage very well but depending on the overall goal everyone can be used. For example, if circuit design target is led to very low consumption power the sub-threshold technique is the most appropriate one However; its low frequency response still remains as before or if the objective of circuit design is with a suitable volume of bulk.

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